REMARKS

Applicant respectfully requests that the Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicant submits that this amendment presents claims in better form for consideration on appeal. Applicant submits that thus there is a good and sufficient reason why this amendment is necessary, why this amendment was not earlier presented, and why this amendment should be admitted now. Furthermore, applicant believes that consideration of this amendment could lead to favorable action that would remove one or more issues for appeal.

Claims 1-6, 8, 9, 13, and 15-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,045,781 to Levy et al. ("Levy").

Claims 7, 10, 11, 12, and 14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Levy.

Claims 1-20 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 09/023172 and claims 1-17 of copending Application No. 09/023234.

Claims 1-20 are pending.

Claims 1, 4, 7, 8-10, and 15-17 have been amended. Applicant respectfully submits that no new matter has been introduced by the amendments made herein.

35 U.S.C. § 102(b) Rejection

The Examiner has rejected claims 1-6, 8, 9, 13, and 15-20 under 35 U.S.C. § 102(b) as being anticipated Levy. In particular, the Examiner states:

Regarding claims 1 and 17-20, Levy shows the claimed system memory controller as memory management unit 22 in Fig. 1, coupled to memory bus 40. This system memory controller handles reads and writes as claimed.

Levy shows the claimed memory module as memory module 30 in Fig. 1. Memory module 30 includes the claimed plurality of memory devices as low stack 0-3 and high stack 0-3. Furthermore, memory module 30 includes the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42. This controller receives a first memory transaction in a first format from the system memory controller and converts it into a second memory transaction in a second format for the plurality of memory devices as claimed. The second memory transaction is clearly different from the first memory format since the outputs of memory transceiver 41 and memory control and timing unit 42 are clearly different from their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures and disclosure.

(pp.2-3 Office Action 8/8/00).

Applicant respectfully submits that claim 1, as amended, is not anticipated by Levy. To anticipate claim 1, Levy must disclose each and every limitation of claim 1. Claim 1 includes the limitations of:

> A system comprising:
> a system memory controller; and
> a first memory module comprising:
> a first plurality of memory devices;
> a first memory module controller coupled to the system memory controller and the first plurality of memory devices, the first memory module controller to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format for the first plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

(Claim 1)(emphasis added).

Levy, however, fails to disclose a first memory module controller coupled to the system memory controller and the first plurality of memory devices, the first memory

module controller to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format for the first plurality of memory devices as recited in claim 1. Levy further fails to disclose that the second format of the second memory transaction is different form the first format of the first memory transaction as recited in claim 1.

Levy, in Figure 1, discloses a memory module 30 coupled to associative memory 24. memory module 30 includes a memory transceiver 41 and memory control and timing circuit 42 coupled to low and high stacks 44 and 45, respectively. The Examiner associates memory transceiver 41 and memory control and timing circuit 42 of Levy with the claimed first memory module controller as recited in claim 1.

The memory transceiver 41 and memory control and timing 42, however, are not related to converting or reformatting a memory transaction in a first format into a memory transaction in a second format. In particular, Levy discloses that:

> . . . During a writing operation, the associative memory 24 transmits BYTE MASK signals (FIG. 5) to the memory control and timing circuit 42 thereby to select one byte or some combination of bytes in the addressed location.
>
> Still referring to FIGS. 1 and 5, the associative memory 24 transmits an ADDRESS PARITY signal which is based upon the value of the address and various control signals that initiate a memory cycle and also data signals if data is being transferred from the associative memory 24. Next the associative memory 24 transmits a START signal that enables the memory control and timing circuit 42 (FIG. 1) to initiate a memory cycle. The circuit 42 transmits back to the associative memory 24 an ACKNOWLEDGE signal that terminates the address and control signals and the BYTE MASK, parity, data and START signals. During a reading memory cycle, the associative memory 24 can initiate another memory cycle with another memory until after the ACKNOWLEDGE signal is terminated.

(Levy Col. 8, lines 41-60).

Thus, Levy teaches that memory control and timing circuit 42 initiates a memory cycle after receiving BYTE MASK and ADDRESS PARITY signals. As such, Levy does not teach that the memory control and timing circuit 42 converts or reformats a first memory transaction into a second memory transaction.

Therefore, for the above reasons, claim 1 is not anticipated by Levy. Given that claims 2-16 depend directly or indirectly on claim 1, claims 2-16 are not anticipated by Levy.

Applicant respectfully submits that claim 17, as amended, is not anticipated by Levy. To anticipate claim 17, Levy must disclose each and every limitation of claim 17. Claim 17 includes the limitations of:

> A system comprising:
> a system memory controller;
> a memory bus coupled to the system memory controller; and
> a memory unit including:
> a plurality of memory devices, and
> a memory module controller coupled to the memory bus and the plurality of memory devices, the memory module controller is to receive a first memory transaction from the memory bus in a first format and is to convert the first memory transaction into a second memory transaction in a second format to at least one of the plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

(Claim 17)(emphasis added).

Levy, however, fails to disclose a system having a memory unit including a plurality of memory devices and a memory module controller coupled to the memory bus and the plurality of memory devices, the memory module controller is to receive a first memory transaction from the memory bus in a first format and

is to convert the first memory transaction into a second memory transaction in a second format to at least one of the plurality of memory devices as recited in claim 17. Levy further fails to disclose that the second format of the second memory transaction is different from the first format of the first memory transaction as recited in claim 17.

As noted above, Levy does not teach converting or reformatting of memory transactions by a memory module controller. Therefore for the above reasons, claim 17 is not anticipated by Levy.

Applicant respectfully submits that claim 18, as amended, is not anticipated by Levy. To anticipate claim 18, Levy must disclose each and every limitation of claim 18. Claim 18 includes the limitations of:

> A method of communicating a memory transaction between a system memory controller and at least one of a plurality of memory devices on a memory module including a memory module controller, the method comprising:
>
> sending a first memory transaction from the system memory controller to the memory module controller, the first memory transaction having a first format;
>
> reformatting the first memory transaction into a second memory transaction for at least one of the memory devices, the second memory transaction having a second format that is different from the first format; and
>
> sending the second memory transaction to the at least one of the memory devices.

(Claim 18)(emphasis added).

Levy, however, fails to disclose a method comprising reformatting the first memory transaction into a second memory transaction for at least one of the memory devices, the second memory transaction having a second format that is different from the

first format and recited in claim 18. Levy further fails to disclose sending the second memory transaction to the at least one of the memory devices as recited in claim 18.

As noted above, Levy does not teach converting or reformatting of memory transactions by a memory module controller. Therefore, for the above reasons, claim 18 is not anticipated by Levy. Given that claims 19-20 depend on claim 18, claims 19-20 are not anticipated by Levy.

35 U.S.C. § 103(a) Rejection

The Examiner has rejected claims 7, 10, 11, 12, and 14 under 35 U.S.C. 103(a) as being unpatentable over Levy. In particular, the Examiner states:

> Regarding claim 7, Levy does not teach that his memory buses operate at different rates, however it would have been obvious to one skilled in the art at the time of the invention to operate them at different rates since they carry different signals and have different lengths, virtually ensuring that the maximum data rate of each one would be different.

(p.6 Office Action 8/8/00).

It is respectfully submitted that the Examiner relies on impermissible hindsight to render claims 7, 10, 11, and 12 obvious. Nowhere in Levy does it disclose or suggest a first memory bus is to operate at a first data rate and the second memory bus is to operate at a second data rate, and wherein the first data rate is different than the second data rate; the first memory bus is to carry time-multiplexed data and address information, and wherein the second memory bus includes separate address and data lines; the first memory module is a dual in-line first memory module (DIMM); and the first memory module is a single in-line first memory module (SIMM) as recited in claims 7, 10, 11, and 12 respectively.

Furthermore, because Levy fails to disclose the limitations of claim 1 and claims 7, 10, 11, and 12 are dependent directly or indirectly on claim 1, claims 7, 10, 11, and

12 are not obvious over Levy. Accordingly, applicant respectfully submits that claims 1-20 are not obvious over Levy and are patentable over the cited art of record.

Double Patenting Rejection

The Examiner has provisionally rejected claims 1-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 09/023172 and claims 1-17 of copending Application No. 09/023234.

Upon a condition of allowance of one or more claims, applicant will submit a timely filed terminal disclaimer.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections have been overcome. Accordingly, applicant requests that claims 1-20 be found in condition of allowance.

If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Mike Kim at (408) 720-8300 x345.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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Sang Hui Michael Kim
Reg. No. 40,450

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300